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IN THE CLAIMS

Please enter the following amendments to the claims. The amendments are believed to introduce no new matter.

What is claimed is:

1. (original) A method for configuring on a programmable chip, the method comprising:

receiving information associated with a primary component, the primary component having either fixed latency or variable latency characteristics;

receiving information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components.

2. (original) The method of claim 1, wherein data, address, and control lines include a data valid line indicating that data is available for transfer from the secondary component.

3. (original) The method of claim 1, wherein the secondary component is operable to receive multiple requests from the primary component before responding.

4. (original) The method of claim 3, wherein the secondary component asserts a wait request line if the secondary component can no longer receive any additional requests.

5. (original) The method of claim 1, wherein the data valid line allows a secondary component read transfer with variable latency.

6. (original) The method of claim 1, wherein a user configures variable latency while selecting the primary and secondary components.

7. (currently amended) The method of claim 1, wherein interconnection circuitry comprises a simultaneous multiple primary component fabric.

8. (original) The method of claim 7, wherein the secondary component is associated with a buffer for holding data available for transfer from the secondary component.

9. (original) The method of claim 8, wherein the primary component is a generic processor module from a component library.

10. (original) The method of claim 9, wherein the secondary component is a generic memory module from a component library.

11. (original) A system for configuring a programmable chip, the system comprising:

an input interface configured to receive information associated with a primary component and information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

a processor configured to generate interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines for the programmable chip, wherein the interconnection module supports a system having both fixed and variable latency components

12. (original) The system of claim 11, wherein data, address, and control lines include a data valid line indicating that data is available for transfer from the secondary component.

13. (original) The system of claim 11, wherein the secondary component is operable to receive multiple requests from the primary component before responding.

14. (original) The system of claim 13, wherein the secondary component asserts a wait request line if the secondary component can no longer receive any additional requests.

15. (original) The system of claim 11, wherein the data valid line allows a secondary component read transfer with variable latency.

16. (original) The system of claim 11, wherein a user configures variable latency while selecting the primary and secondary components.

17. (original) The system of claim 11, wherein interconnection circuitry comprises a simultaneous multiple primary component fabric

18. (original) The system of claim 17, wherein the secondary component is associated with a buffer for holding data available for transfer from the secondary component.

19. (original) The system of claim 18, wherein the primary component is a generic processor module from a component library.

20. (original) The system of claim 19, wherein the secondary component is a generic memory module from a component library.

21. (original) A computer readable medium comprising computer code for configuring a programmable chip, the computer readable medium comprising:

computer code for receiving information associated with a primary component, the primary component configurable as either a fixed latency or a variable latency component;

computer code for receiving information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

computer code for generating interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module support a system having both fixed and variable latency components.

22. (original) The computer readable medium of claim 21, wherein data, address, and control lines include a data valid line indicating that data is available for transfer from the secondary component.

23. (original) The computer readable medium of claim 21, wherein the secondary component is operable to receive multiple requests from the primary component before responding.

24. (original) The system of claim 23, wherein the secondary component asserts a wait request line if the secondary component can no longer receive any additional requests.

25. (original) The computer readable medium of claim 21, wherein the data valid line allows a secondary component read transfer with variable latency.

26. (original) The computer readable medium of claim 21, wherein a user configures variable latency while selecting the primary and secondary components.

27. (original) The computer readable medium of claim 21, wherein interconnection circuitry comprises a simultaneous multiple primary component fabric.